

# Characterization of RF-IC Packages by Multiport Excitation

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*Abstract*— A new measurement technique based on multiport TDR excitation is presented. The technique is quite accurate and is used to characterize low-cost and small lead frame plastic packages. The extracted self and mutual inductance and capacitance values of a typical package are presented.

## I. INTRODUCTION

Design of wireless circuits and systems includes low-noise amplifiers, oscillators, filters, couplers and other mixed signal modules. The effects of package parasitics, the self and mutual coupling elements and isolation across package pins, should be incorporated into the design cycle to address issues such as frequency pulling of oscillator circuits, stability of amplifier circuits, and crosstalk noise. A number of electromagnetic simulation and measurement based techniques have been proposed in recent years for the characterization of RF analog and high speed digital packages. Techniques to characterize multiple coupled interconnects associated with these packages by using time domain multiport reflection measurements and multi-dimensional deconvolution (peeling) algorithms have also been developed [1-3]. These algorithms extract coupled line nonuniform impedance profiles associated with the package interconnects and are readily implemented with transmission line or other compatible fixtures for accessing the package pins. These models are converted to coupled lumped element models by integrating the characteristic impedance and admittance matrix elements.

Application of multi-dimensional deconvolution procedure to small packages with electrically short pins is dependent on the deembedding procedure which can become insensitive, particularly if the fixture lines are electrically long and coupled. A new and sensitive measurement technique, capable of charac-

terizing packages with electrically short pins, is developed in this paper. The technique is based on multichannel excitation of TDR pulses and is used to extract the self and mutual inductances and capacitances of low-cost and small lead frame RF wireless IC packages. In addition, only a one-dimensional peeling algorithm is required to extract the circuit elements. The extracted circuit element values for a typical SOIC package from measurements are presented.

## II. THE EXTRACTION PROCEDURE

The technique is demonstrated by the characterization and modeling of typical small pin count SOIC RF packages, such as the one shown in Figure 1, by utilizing microstrip line fixtures. Figure 2 shows the transmission line fixture used. This fixture is also used to measure the isolation between package pins that are across from each other. By exciting four successive pins in two different configurations, with identical magnitude TDR step waveforms, the middle two pins are characterized. The two types of excitations are shown in Figure 3. In one case, all four pins are excited with the same polarity of step voltages from a multichannel TDR system. In the second case, the polarity of the step voltages of the first two pins is reversed. The technique requires that all the steps reach the end of the test fixture at the same time. The excitations are chosen so that selected pins are isolated, facilitating the extraction of their self and mutual inductances and capacitances by establishing reference planes. It should be noted here that these excitations do not in general correspond to the normal modes of the coupled system. The TDR voltages of the two middle pins are recorded in the two types of excitations.

The impedance and admittance profiles of each channel for both types of excitation are obtained by applying the one-dimensional peeling algorithm. The

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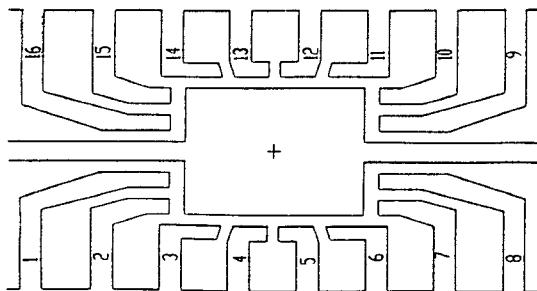


Fig. 1. The lead frame of a 16 pin SOIC package.

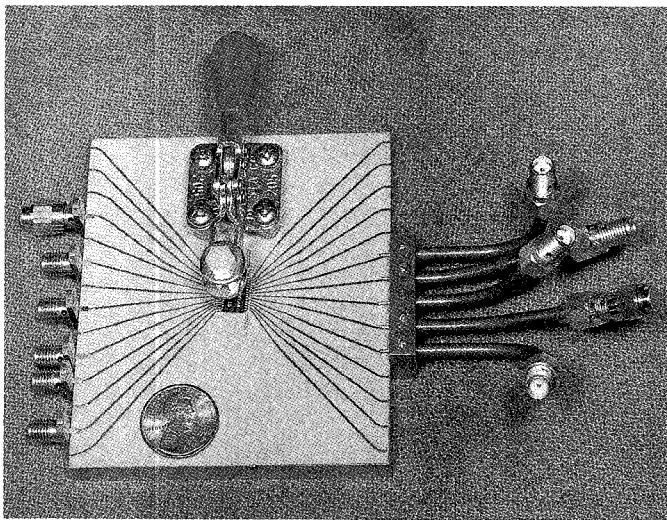


Fig. 2. Fabricated test fixture for package characterization.

inductance and capacitance seen by each pin is obtained by integrating the impedance profile and the admittance profile, respectively. From these the self and mutual inductances and capacitances associated with each pin can be calculated. For example, the calculation of self and mutual capacitances is illustrated in Figure 3. The capacitances seen by pins in the same polarity excitation are the pin capacitances to ground. The capacitances seen by pins in the opposite polarity excitation are the sum of pin capacitances to ground and twice the mutual capacitance

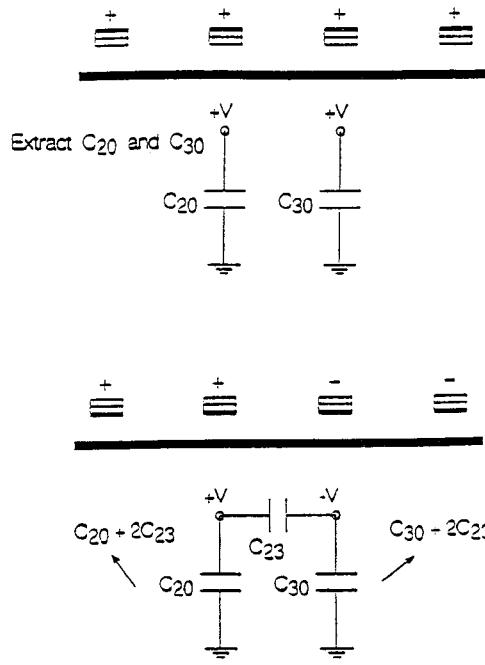


Fig. 3. The two types of excitations and the capacitances seen by the pins.

between the two pins. Since the pin capacitances to ground are already known from the first type of excitation, the mutual capacitance between the pins can be found. In a similar manner, the self and mutual inductances can also be calculated. The equivalent circuit for the extraction of self and mutual inductances is shown in Figure 4. Let  $L_{2+}$ ,  $L_{3+}$  and  $L_{2-}$ ,  $L_{3-}$  be the inductances seen at pins 2 and 3 with the same polarity and opposite polarity excitations, respectively. These can be expressed in terms of the self and mutual inductances of pins 2 and 3 shown in Figure 4.

$$L_{2+} = \frac{L_2 L_3 + L_{23}(L_2 + L_3)}{L_3} \quad (1)$$

$$L_{3+} = \frac{L_2 L_3 + L_{23}(L_2 + L_3)}{L_2} \quad (2)$$

$$L_{2-} = \frac{L_2 L_3 + L_{23}(L_2 + L_3)}{(L_3 + 2L_{23})} \quad (3)$$

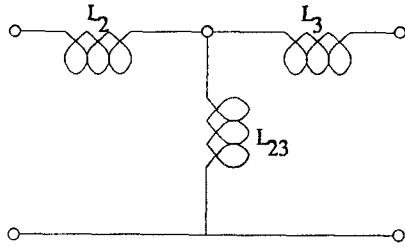


Fig. 4. Equivalent circuit for extraction of inductors.

$$L_3^- = \frac{L_2 L_3 + L_{23}(L_2 + L_3)}{(L_2 + 2L_{23})} \quad (4)$$

From these relations,  $L_2$ ,  $L_3$  and  $L_{23}$  can be found. There are three unknowns and four relations for both capacitances and inductances. The fourth relation can be used to check the accuracy of the values. Typically, the mutual capacitances and inductances beyond the nearest neighbor are small. However, if desired, these can be measured in the same manner in defined configurations. In general, to characterize each additional off-diagonal term, the number of exciting channels need to be increased by one. In this way, the complete  $[L]$  and  $[C]$  matrix elements of the IC package can be extracted. The procedure to extract the second nearest neighbor mutual capacitance by excitation of five channels in three different configurations is illustrated in Figure 5.

### III. MEASUREMENTS

Measurements are made on both empty packages and packages with die and bond wires connected to die pads. Measurement of the test fixture alone is also performed to characterize the test fixture itself. Figure 6 shows the typical waveforms for the two types of excitations. The extracted capacitances and inductances of the package shown in Figure 1 are shown in Table 1. Due to the limited dynamic range of the sampling scope, a network analyzer is used to measure the isolation between pins that are across the package. The same test fixture is also used for isolation measurements. The isolation capacitance is found by optimization of the circuit shown in Figure 7. The self capacitance and inductance of the pins are known from the TDR measurements and the isolation capac-

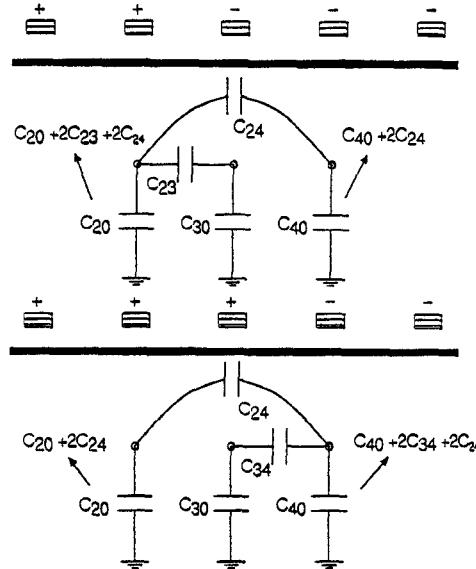


Fig. 5. Extraction of second nearest neighbor capacitance from excitation of five pins.

itance is found by optimization. The measured and fitted  $S_{21}$  of an 8-pin SOIC package are also shown in Figure 7. The measured inductances and capacitances are compared with the calculated ones using FastHenry [4] and FastCap [5] and good agreement is found.

### IV. CONCLUSION

A new measurement technique to characterize the electrically short RF-IC packages is described and typical results are presented. This technique requires the application of only one-dimensional peeling algorithm and both self and mutual elements are extracted. The lumped element models can be used at RF frequencies of up to about 5 GHz. The distributed or hybrid models are required at higher frequencies [2].

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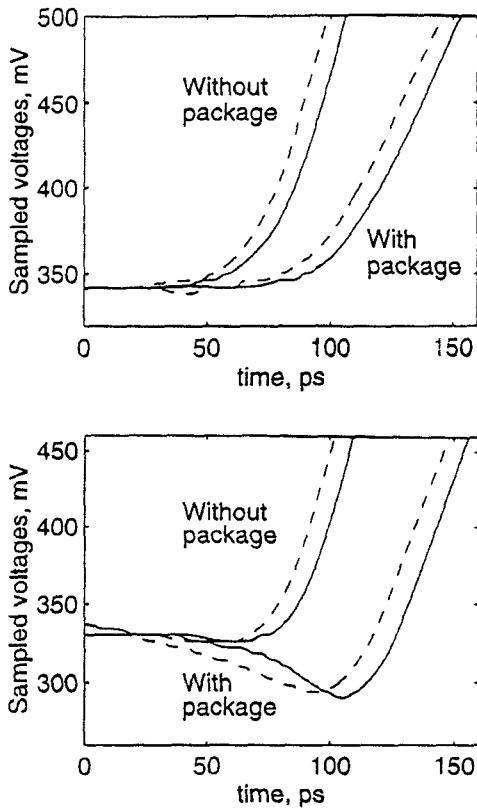


Fig. 6. TDR waveforms of two middle pins. a) Same polarity excitation, b) Opposite polarity excitation (In the plot the negative TDR step is plotted as positive for comparison)

Table 1. Extracted self and mutual capacitances and inductances of a 16-pin SOIC package. The rest can be found from symmetry. (The capacitances are in pF and the inductances are in nH)

Capacitances element	Without bond wires	With bond wires
C11	0.487	0.622
C22	0.336	0.459
C33	0.192	0.315
C44	0.151	0.237
C12	0.074	0.097
C13	0.034	0.043
C14	0.015	0.036
C15	0.015	0.035

Inductance element	Without bond wires	With bond wires
L11	1.370	1.758
L22	1.003	1.375
L33	0.636	0.960
L44	0.428	0.744
L12	0.232	0.329
L13	0.111	0.160
L14	0.059	0.123
L15	0.053	0.121

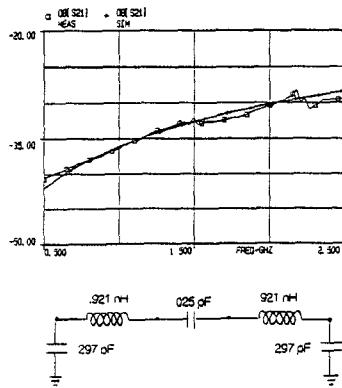


Fig. 7. Extracted equivalent circuit for pins 4 and 5 of 8-pin SOIC package for isolation (opposite end crosstalk) and plot of measured and equivalent circuit  $S_{21}$

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